CLAIM LISTING:

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A buffer circuit comprising:

a plurality of memory locations to hold data;

~~the memory locations of the plurality of memory locations addressable across an address space;~~

a read pointer to point a read address of the plurality of memory locations from which to read output data;

a write pointer to point a write address of the plurality of memory locations in which to write input data;

the read pointer and the write pointer[[s]] operable responsive to a ~~respective~~ read clock signal and a write clock[[s]] signal, respectively, to sequence the read address and the write address[[es]], respectively, across ~~the~~ an address space of the plurality of memory locations;

a control register to store a nominal level ~~as a set fill level~~ for ~~of~~ the buffer circuit;

the control register being programmable for receiving the nominal level for setting latency of the read pointer;

the latency of the read pointer being variable responsive to a fill level of the plurality of memory locations relative to the nominal level; and

a controller to affect operation of the read pointer dependent on the write address of the write pointer, the read address of the read pointer, and the nominal level[[;]]

~~the controller configured to controllably activate and deactivate operation of the read pointer by electrically coupling and decoupling, respectively, a clock input of the read pointer for obtaining the read clock~~.

2. (Currently Amended) The buffer circuit of claim 1, the controller operable to:

determine an amount of data in the buffer circuit based on a difference between the write address and the read address; and

~~enable~~ cause the read pointer to increase the read address in advance of the read clock signal responsive to the amount of data being greater than the nominal level; ~~based on a difference between the amount of data determined and the nominal level~~

wherein the controller is configured to adjust the read pointer independently of the read clock signal.

3. (Currently Amended) The buffer circuit of claim 2, in which the controller is further operable to ~~at least~~ hold the read address of the read pointer when the amount of data is determined to be less than the nominal level.

4. (Currently Amended) The buffer circuit of claim 2, in which the controller is further operable to decrement the read address in advance of the read clock signal when the amount of data is determined to be less than the nominal level.

Claims 5-8. (Cancelled)

9. (Currently Amended) The buffer circuit of claim 1, further comprising initialization circuitry to:

configure the write pointer with a predetermined start address for the write address; and

configure the read pointer with a beginning value based on the predetermined start address for the write address and the nominal level.

10. (Currently Amended) The buffer circuit of claim 9, in which the beginning address for the read pointer is an address offset from the starting write address, and the address offset is equal to the nominal level.

Claims 11-43. (Canceled)